**Digital Design (CSCE 2114) – Lab 8**

In this lab you are to write VHDL code to implement a Moore type state machine.

The state machine implements a 2-bit binary up counter. It has the following inputs and outputs:

Clk (input) - the clock input

Rstn (input) - an active low asynchronous reset that holds the outputs to 00 for as long as it is low

Enable (input) - an active high enable signal, when it is high the counter is enabled, when it is low the counter stops and maintains its present count value

Count (output) – this is a two bit vector that is the count pattern output

As long as Rstn and Enable are both 1 the counter will cycle through the count pattern 00, 01, 10, 11, then it repeats. As described above Rstn is an asynchronous active low reset. If Rstn is low the count pattern will immediately go to 00 regardless of the other input values. The Enable input is active high, if it is a 1 the counter is enabled to count. If Enable is low the counter will stop with its present count value unless Rstn is 0. If Enable is low the count pattern will stop but if Rstn then goes low the count pattern will go to 00.

The state machine has 2 outputs, a Rstn input (active low), an Enable input (active high), and a Clk input (rising edge triggered). Rstn is an asynchronous reset that resets to the outputs to 00 when Rstn is low. If Rstn and Enable are high, the state machine cycles through a binary count pattern from 00 to 11, then turns back over to 00 and repeats. If Rstn is low the outputs are 00 regardless of the value of Enable or Clk values or transitions.

Steps:

1. Create a new project and VHDL file. It’s best not to use the default project directory that Quartus lists. Name the project file, VHDL file, and entities (in the code) the same name.
2. After finishing your code, compile your project and correct any errors.
3. Add a waveform file and set valid test data for the input signals. Use a 50ns clock period. Run the simulation and check the output/results. List the inputs and outputs in the order they are listed above. To make your report clear you may need to use more than one image of your simulation results. Make sure that they are readable.
4. Remember to save your results (waveforms) and explain them in your lab report.

Report:

Prove that you tested the design to show proper functionality. Make sure you test the count pattern, the Rstn input, and the Enable input for all possible combinations that are meaningful. You should include your VHDL code, a state diagram, simulation waveforms, and describe what was tested for the clock periods of your simulation. Include any narrative that is necessary to document your design and its correct functionality.